

Appl. No. 10/711,197  
Amdt. dated January 06, 2006  
Reply to Office action of December 06, 2005

**Amendments to the Claims:**

1. (Original) A method for fabricating a dual-bit non-volatile memory cell, the method comprising:

- forming a dummy gate, having an upper surface and two sidewalls, on a substrate;
- 5 forming a stack of layers, having at least an oxide silicon layer and a silicon nitride layer overlying the oxide silicon layer, on the upper surface and two sidewalls of the dummy gate and exposed portions of the substrate;
- forming a dummy oxide overlying the stack of layers;
- 10 etching a portion of the dummy oxide, a portion of the stack of layers on the two sidewalls of the dummy gate, and a portion of the dummy gate using a first etching process, wherein the bottom of the silicon nitride layer is utilized as a stop layer;
- removing the dummy gate such that the stack of layers has a first opening to expose a portion of the substrate;
- 15 forming a gate oxide layer on the first opening such that the gate oxide layer has a recess within the first opening;
- forming a first polysilicon layer on the gate oxide layer;
- forming a control gate on the recess using the first polysilicon layer;
- forming a second oxide silicon layer on the surface of the control gate and the stack
- 20 of the layers;
- forming a second polysilicon layer on the second oxide silicon layer; and
- performing a self-aligned etching to anisotropically etch the second polysilicon layer to form dual split-gates on the second oxide silicon layer, separated from the control gate by the second oxide silicon layer.
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2. (Original) The method of claim 1 wherein portions of the dummy oxide, the stack of layers, and the dummy gate are removed before the first etching process.

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3. (Original) The method of claim 2 wherein removal of the portions of the dummy oxide, the stack of layers, and the dummy gate before the first etching process is performed by chemical mechanical polishing (CMP).
- 5 4. (Original) The method of claim 2 wherein removal of the portions of the dummy oxide, the stack of layers, and the dummy gate before the first etching process is performed by etching back.
- 10 5. (Original) The method of claim 1 wherein the bottom of the silicon nitride layer is defined as being on and substantially parallel to the substrate.
6. (Original) The method of claim 1 wherein the substrate comprises a drain region and a source region, each of the regions uniquely corresponding to one of the split-gates.
- 15 7. (Original) The method of claim 1 wherein the dummy gate is formed using a mask used for forming the control gate.
8. (Original) The method of claim 1 wherein the first etching process is performed by dry etching.
- 20 9. (Original) The method of claim 1 wherein the dummy gate is made from silicon dioxide.
- 25 10. (Withdrawn) A dual-bit non-volatile memory cell, the dual-bit non-volatile memory cell comprising:  
a stack of layers on a surface of a substrate, the substrate having at least one first oxide silicon layer and a silicon nitride layer overlying the first oxide silicon layer, the stack of layers having an opening exposing a portion of the substrate;

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a gate oxide layer on the surface of the substrate within the opening;  
a control gate on the gate oxide layer;  
a second oxide silicon layer overlying a portion of the surface of the control gate,  
a portion of the gate oxide layer, and the stack of layers; and  
5 dual split-gates on the second oxide silicon layer, separated from the control gate  
by the second oxide silicon layer.

11. (Withdrawn) The dual-bit non-volatile memory cell of claim 10 wherein the substrate  
comprises a drain region and a source region, each of the regions uniquely  
10 corresponding to one of the split-gates.